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(54) Low power consumption linear voltage regulator having a fast response with respect to the load transients

(57) A linear type of voltage regulator, having at least one input terminal (VBAT) adapted to receive a supply voltage and one output terminal (VOUT) adapted to deliver a regulated output voltage, comprises a power transistor (M1) and a driver circuit for the transistor; the driver circuit comprises essentially an operational amplifier (OP1) having an input differential stage biased by a bias current which varies proportionally with the variations of the regulated output voltage at the output terminal (VOUT) of the regulator.

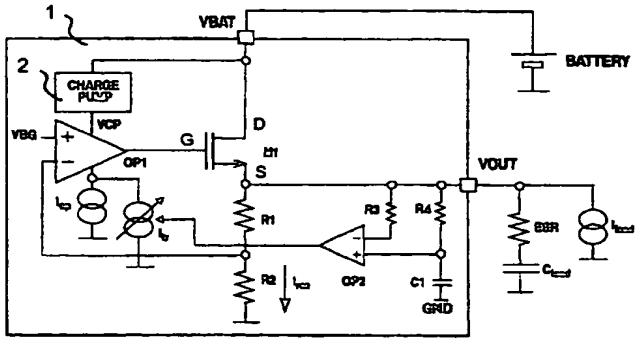

FIG.2

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Description

This invention relates to a linear type of voltage regulator.

Field of the Invention

In particular, the invention relates to a linear type of voltage regulator controlled for optimum power consumption and useful with battery-powered portable devices.

Such regulators must exhibit very fast response to load transients, low voltage drop, high rejection to the supply line, and above all, low current consumption so that the battery charge can be made to last longer.

Background Art

Current regulators are implemented using an n-channel MOS power transistor. The reason for preferring an n-channel transistor is that, for a given performance level, it allows the occupation of silicon area to be optimized and the value of the output capacitor to be reduced by at least one order of magnitude.

An examplary application of a conventional type of voltage regulator is illustrated in Figure 1.

A regulator of the low-drop type having an n-channel topology, such as that shown in Figure 1, requires a driver circuit OP1 being supplied a higher voltage, VCP, than the supply voltage, VBAT, a feature which has been achieved in state-of-art regulators by using a charge pump circuit 2.

The operation of the device in the circuit of Figure 1 and its application will now be described in detail.

The current consumption of the regulator can be calculated from the current I_{res} being flowed through the divider R1-R2 plus the current draw I_{op} of the driver circuit OP1 for the power transistor M1.

Since the charge pump circuit 2 used for powering the driver circuit OP1 is a multiplier-by-n of the input voltage VBAT, its current draw from the battery is n times the current I_{op} that it delivers to the driver circuit OP1.

Considering, moreover, the efficiency E_{ff} of the charge pump circuit, the overall battery current consumption of the regulator is:

$$I_{REG} = n/E_{ff} * I_{op} + I_{res}.$$

The compensation usually employed for a regulator with this topology is of the pole-zero type, where the internal zero is to cancel out the pole introduced by the load capacitor.

The outcome of such compensation is that a dominant pole is obtained, which considerably slows the response to load transients and produces a large output voltage variation.

A prior solution to this problem consists of increasing the bias current I_{op} of the differential stage of the driver circuit OP1, with the consequence of increasing the overall consumption of the regulator.

This solution clashes, however, with the main characteristic of battery-powered devices, whose current consumption is to be kept as low as possible.

The underlying technical problem of this invention is to provide a voltage regulator of the linear type controlled for otpimum current consumption, which can exhibit fast response to the load transients and minimize the average consumption of the regulator.

The technical problem is solved by a circuit as indicated and defined in the characterizing parts of Claims 1 to 7.

Summary of the Invention

The solvent idea on which the present invention is based is one of using a driver circuit OP1 for the power transistor M1 which has an input differential stage biased by a bias current that varies proportionally with the variations in the output voltage V_{OUT}.

The features and advantages of the circuit according to this invention will be more clearly apparent from the following detailed description of embodiments thereof, shown by way of non-limitative example in the accompanying drawings.

Brief Description of the Drawings

Figure 1 shows a linear type of voltage regulating circuit according to the prior art;

Figure 2 shows a linear type of voltage regulating circuit according to this invention;

Figure 3 shows a first embodiment of a portion of the voltage regulating circuit in Figure 2;

Figure 4 shows a second embodiment of a portion of the voltage regulating circuit in Figure 2; and

Figure 5 shows plots versus time of some voltage and current signals, as obtained by electrical simulation of the circuit in Figure 2.

Detailed Description

Shown in Figure 2 is a voltage regulating circuit 1 of the linear type which embodies this invention.

The regulating circuit 1 is connected between a battery (BATTERY), itself connected to a terminal VBAT of the circuit, and a load which is connected to a terminal VOUT and illustrated schematically by a generator of an equivalent current I_{load} in parallel with a load capacitor C_{load} having an equivalent series resistor ESR.

The following circuit components make up the regulating circuit 1:

a power transistor M1 of the n-channel MOS type having a main drain-source conduction path connected between the terminals VBAT and VOUT of the circuit 1;

an operational amplifier OP1 which is used as a driver circuit for the power transistor M1, has an input differential stage biased by a certain bias current I_{op}, a non-inverting input terminal connected to a voltage reference VBG, an inverting input terminal coupled to the output terminal VOUT of the circuit 1 through a resistive divider R1-R2, and an output terminal connected to the control terminal G of the power transistor M1;

a charge pump circuit 2 used for powering the operational amplifier OP1;

a transconductance operational amplifier OP2, I_{tr} having an inverting (-) input terminal coupled to the output terminal VOUT of the regulator through a resistor R3, and a non-inverting (+) input terminal coupled to the output terminal VOUT of the regulator through a low-pass filter C1, R4.

The low-pass filter comprises a resistor R4 connected between the regulator output terminal VOUT and the non-inverting (+) input of the transconductance operational amplifier OP2, and a capacitor C1 connected between the non-inverting (+) input of the amplifier OP2 and a fixed voltage reference GND.

The operation of the circuit shown in Figure 2 will now be described.

As the load current I_{load} goes from a minimum value to a maximum value, for example, the output voltage VOUT begins to drop due to the slow driving of the transistor M1 by the operational amplifier OP1.

This variation in the output voltage VOUT reflects immediately on the inverting (-) input of the transconductance operational amplifier OP2, whereas the voltage at the non-inverting input is filtered by the low-pass filter network R4-C1.

Under this condition, the output of the transconductance operational amplifier OP2, consisting of a driven current generator, designated I_{tr} in the Figure, affects the bias current of the input differential stage of the operational amplifier OP1, increasing its value. In fact, the current I_{tr} adds to the bias current I_{op} of the operational amplifier OP1 in the rest condition.

Thus, the overall bias current of the input differential stage of the operational amplifier OP1, driving the power transistor M1, will the higher the larger is the variation in the voltage applied to the output terminal VOUT of the regulator, thereby enhancing the speed of response of the circuit.

Accordingly, the current consumption of the regulator will only increase during those load transients which induce variations in the value of the output voltage VOUT. On termination of the transient, the inputs of the operational amplifier OP2 return to the same potential, restoring the current generator I_{tr} to its very low or zero initial value.

The proposed solution has been implemented using BCD (Bipolar-CMOS-DMOS) technology.

Figure 3 shows diagramatically a circuit, generally referenced 3, of a first embodiment of the transconductance operational amplifier OP2, I_{tr} using bipolar transistors.

The circuit 3 comprises an input differential stage consisting of transistors Q1, Q2, Q3, Q4, a generator of a reference current I_{ref}, and an output current mirror Q5, Q6.

Assuming that all the (npn and pnp) transistors are of unity area, in a condition of constant load, the current I_{tr} will be equal to I_{ref}.

If the output voltage VOUT tends to drop, due to a load transient, the voltage at the base of Q2 immediately follows the voltage VOUT, while the base voltage of Q1 decreases at a time constant equal to R4*C1. Under this condition, the collector currents of Q1 and Q4 increase, resulting in an increased output current I_{tr}.

Calling ΔV the voltage variation at the output VOUT, the current I_{tr} is given by:

$$I_{tr} = I_{ref} * {}_{e}\Delta V/(1+\eta)*V_T$$

where η is the emission coefficient of the transistors Q3 and Q4.

When the voltage transient at the output VOUT terminates, and the voltages at the bases of the transistors Q1 and Q2 revert to the same potential, the collector currents of Q1 and Q2 are returned to a balanced condition and, accordingly, the current Itr decreases to its initial value I_{ref}.

Thus, when using the circuit of Figure 3, the bias current will only increase as the output voltage VOUT tends to drop.

The steady state consumption is of 3 microAmperes for the circuit of Figure 3, and is obtained from a reference current I_{ref} of 1 microAmpere.

The consumption of the operational amplifier OP1 amounts to about 4 microAmperes; considering that this amplifier is supplied a boosted voltage VCP from the charge pump circuit 2, and that the circuit 2 is a voltage tripler, the current drawn from the battery will be 4*3=12 microAmperes.

The current I_{res} flowing through the divider R1-R2 is 4 microAmperes.

Therefore, the regulator overall consumption will amount approximately to 16 microAmperes.

On the other hand, when using a conventional type of circuit, such as that shown in Figure 1, the overall consumption in the steady state condition would be about 45 microAmperes, for a like performance in terms of response to load transients.

The subject circuit solution can be extended to

include applications where a fast response to both connections and disconnections of the load is demanded, that is even where the load current on the voltage regulator may decrease sharply or, upon disconnection of the load, drop to zero.

Figure 4 shows a second embodiment, generally referenced 4, of the transconductance operational amplifier OP2, I_{tr}, which is also implemented by bipolar transistors.

The circuit 4 comprises a double input differential stage consisting of transistors Q1, Q2, Q3, Q4, Q5, Q6, two generators of reference currents I_{ref1} and I_{ref2}, and an output current mirror Q7, Q8.

The differential stage is arranged such that the transistor pair Q3 and Q4 amplify the current I_{ref1} on the occurrence of a negative transient of the voltage VOUT, similar to the circuit of Figure 3, while the transistor pair Q5 and Q6 amplify the current I_{ref2} on the occurrence of a positive transient of the voltage VOUT.

Assuming unity area for all (npn and pnp) transistors, in a condition of constant load, the current I_{tr} will be $I_{ref}=I_{ref1}+I_{ref2}$.

If the output voltage VOUT tends to drop, due to a sharp increase in the load current, the base voltage of the transistor Q2 also drops immediately, following the voltage VOUT, while the base voltage of Q1 decreases at a time constant equal to R4*C1. Under this condition, the collector currents of Q1 and Q4 will increase and result in the output current I_{tr} being also increased.

On the other hand, if the output voltage VOUT increases, due to a sharp decrease in the load current, then the base voltage of the transistor Q2 increases immediately, following the voltage VOUT, while the base voltage of Q1 increases at a time constant equal to R4*C1. In this case, the collector currents of Q2 and Q6 will increase and result in the output current I_{tr} being also increased.

In this way, the current I_{tr} is increased whenever positive or negative variations occur in the output voltage VOUT of the regulator.

Figure 5 shows plots of the output voltage VOUT, graph (a), and the current I_{tr}, graph (b), as obtained by electrical simulation of the circuit.

The signal VOUT pattern obtained when using this circuit, curve 41, overlaps the pattern of the same signal, curve 40, when this circuit is not used; the different voltage drop across the signal is quite apparent.

It will be appreciated that this operating priciple can also be used with regulators having different topologies.

The advantages of this solution can be summarized as follows:

- improved speed of response to transients of the differential stage of a linear regulator;
- low average current consumption.

Claims

1. A linear type of voltage regulator having at least one input terminal (VBAT) adapted to receive a supply voltage and one output terminal (VOUT) adapted to deliver a regulated output voltage, comprising:

   a power transistor (M1) having a control terminal (G) and a main conduction path (D-S) connected between the input terminal (VBAT) and the output terminal (VOUT) of the regulator;

   an operational amplifier (OP1) having an input differential stage biased by a bias current, and having a first input terminal connected to a voltage reference (VBG), a second input terminal coupled to the output terminal (VOUT) of the regulator, and an output terminal connected to the control terminal of the power transistor (M1);
   characterized in that the bias current of the differential stage varies proportionally with the variations of the regulated output voltage at the output terminal (VOUT).

2. A voltage regulator according to Claim 1, characterized in that the bias current of the differential stage of the operational amplifier (OP1) is the sum of a first current (I_{op}) from a constant current generator plus a second current (I_{tr}) from a tranconductance operational amplifier (OP2) having at least one input terminal coupled to the output terminal (VOUT) of the regulator.

3. A voltage regulator according to Claim 2, characterized in that the transconductance operational amplifier (OP2) has an inverting (-) input terminal coupled to the output terminal (VOUT) of the regulator through a resistor (R3), and a non-inverting (+) input terminal coupled to the output terminal (VOUT) of the regulator through a low-pass filter.

4. A voltage regulator according to Claim 3, characterized in that the low-pass filter comprises a resistor (R4) connected between the output terminal (VOUT) of the regulator and the non-inverting (+) input of the transconductance operational amplifier (OP2), and a capacitor (C1) connected between the non-inverting (+) input of said amplifier (OP2) and a fixed voltage reference (GND).

5. A voltage regulator according to Claim 4, characterized in that the power transistor (M1) is an n-channel MOS transistor.

6. A voltag regulator according to Claim 5, characterized in that the operational amplifier (OP1) is sup-

plied a boosted voltage (VCP) above the supply voltage (VBAT).

7. A voltage regulator according to Claim 6, characterized in that the first input terminal of the operational amplifier (OP1) is a non-inverting (+) input terminal, and the second input terminal is an inverting (-) input terminal coupled to the output terminal (VOUT) of the regulator through a voltage divider (R1-R2).

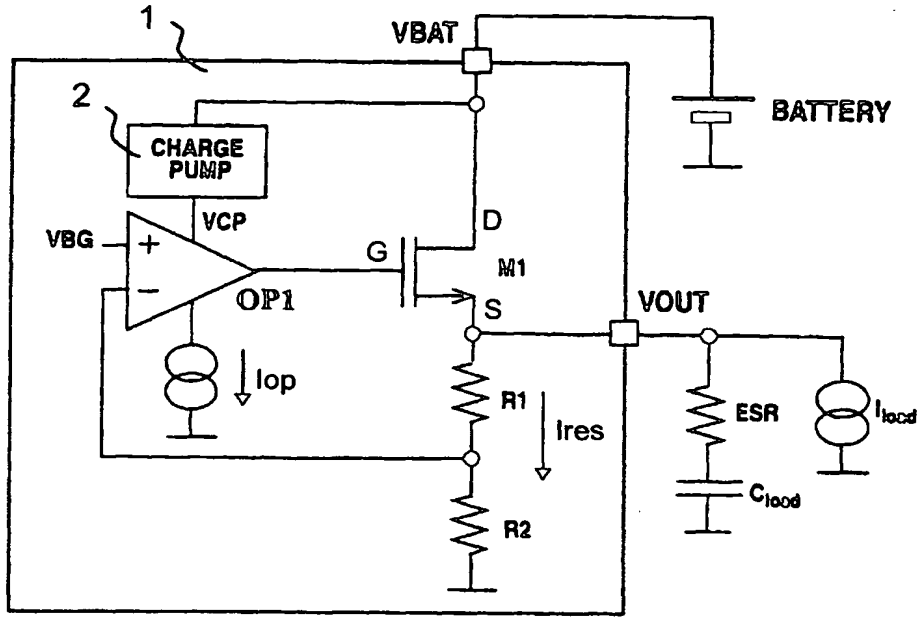
1
VBAT
2
CHARGE PUMP
BATTERY
VCP
VBG
D
G
M1
OP1
S
VOUT
Iop
R1
Ires
ESR
Iload
Cload
R2

FIG.1

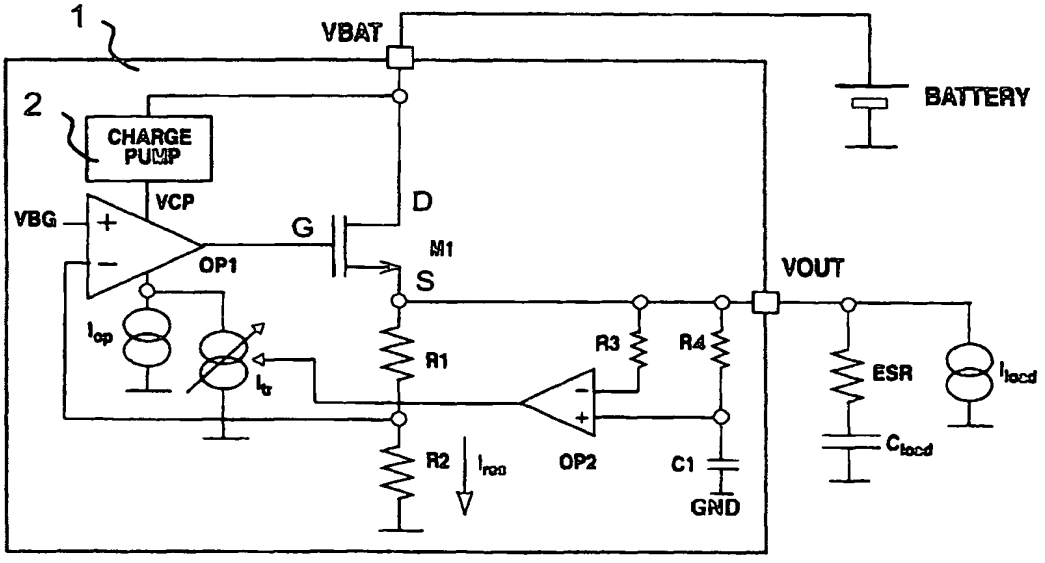
1
VBAT
2
CHARGE PUMP
BATTERY
VCP
VBG
D
G
M1
OP1
S
VOUT
Iop
Ir
R1
R3
R4
ESR
Iload
Cload
R2
Ires
OP2
C1
GND

FIG.2

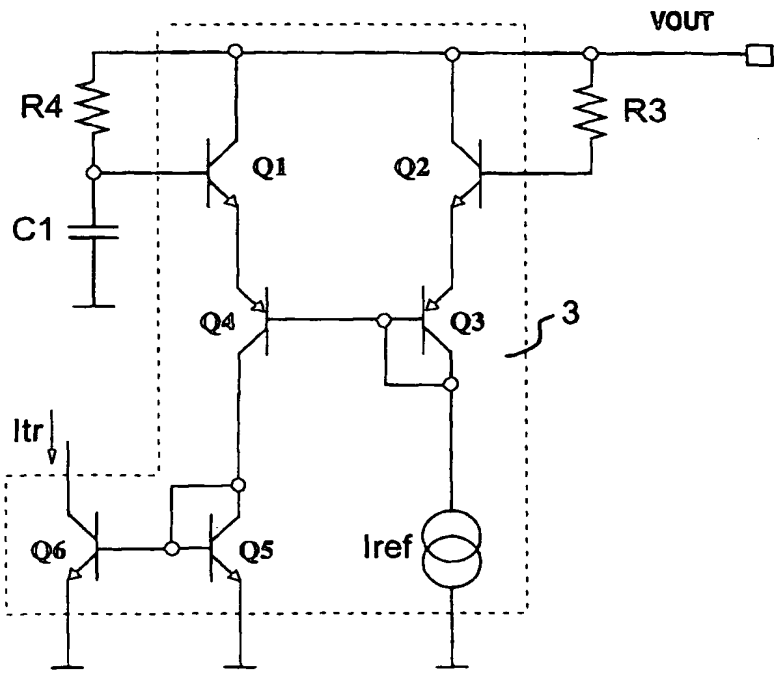
VOUT
R4
R3
Q1
Q2
C1
Q4
Q3
3
Itr
Q6
Q5
Iref

FIG.3

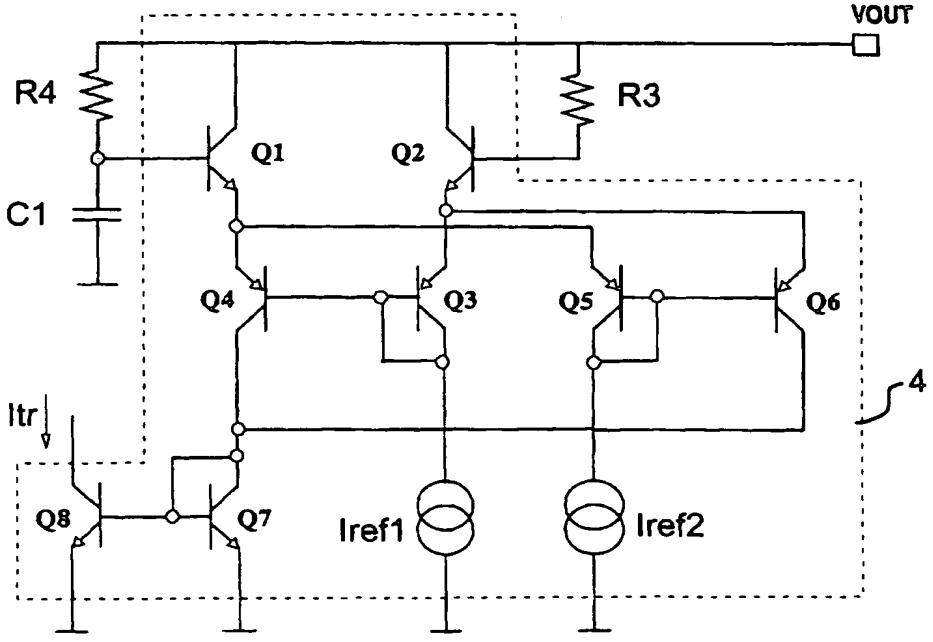
VOUT
R4
R3
Q1
Q2
C1
Q4
Q3
Q5
Q6
4
Itr
Q8
Q7
Iref1
Iref2

FIG.4

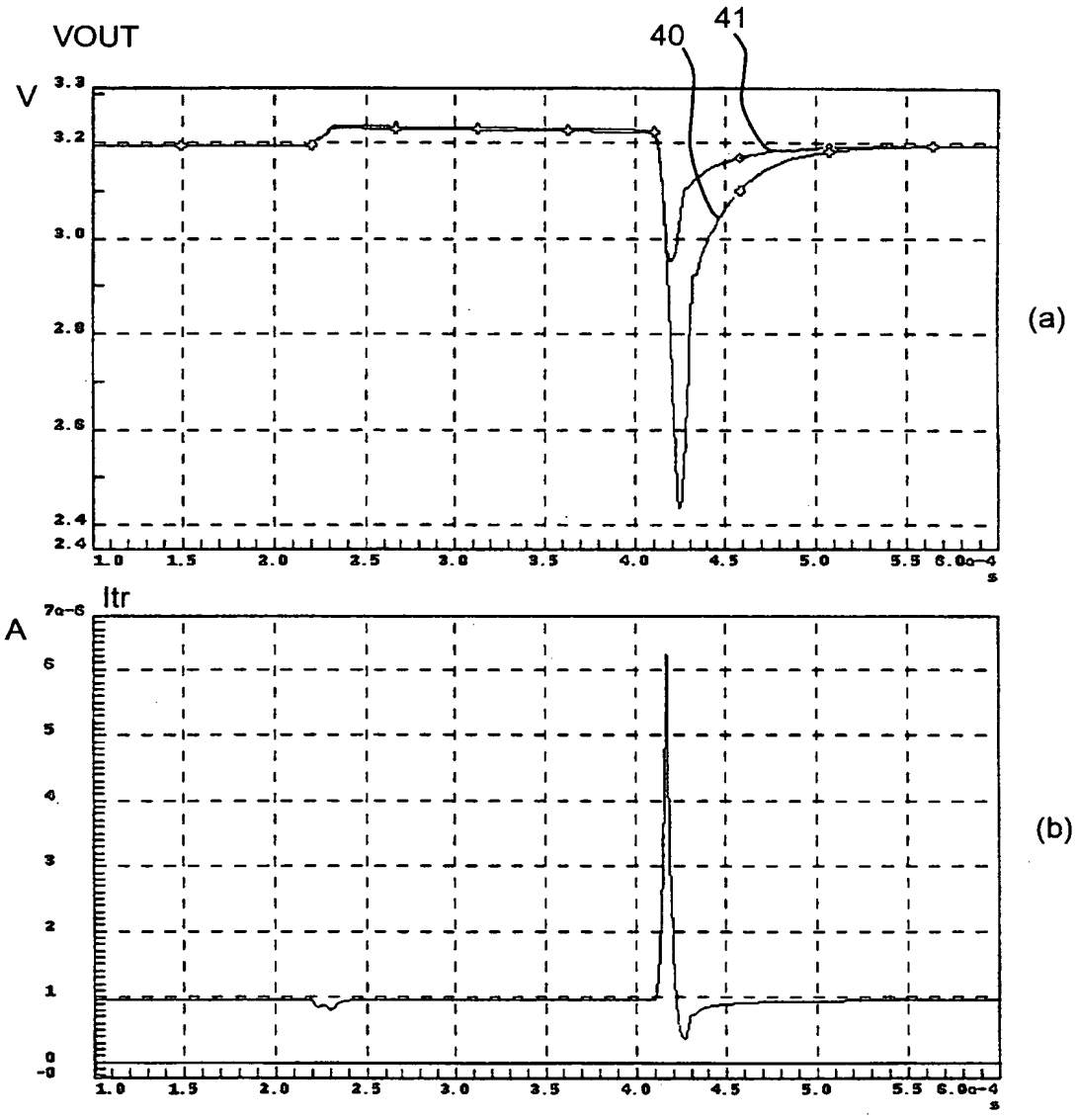
VOUT
40
41
V
3.3
3.2
3.0
2.8
2.6
2.4
2.4
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0e-4
s
(a)
Itr
A
7e-6
6
5
4
3
2
1
0
-0
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0e-4
s
(b)

FIG.5

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EUROPEAN SEARCH REPORT

Application Number
EP 97 83 0348

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 548 205 A (MONTICELLI DENNIS M) * column 5, line 2 - line 65; figure 4 *	1,2	G05F1/565
X	US 4 906 913 A (STANOJEVIC SILVO) * column 6, line 50 - line 68; figure 2 *	1,2	
A	EP 0 742 509 A (NOKIA MOBILE PHONES LTD) * abstract; figure *	1	
A	EP 0 476 365 A (MOTOROLA JAPAN) * abstract; figure * * column 1, line 29 - line 50 *	1-7	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G05F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18 December 1997	Lampe, S

CATEGORY OF CITED DOCUMENTS

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